YASKAWA

ANTAIOS
Evaluation Kit
User Guide

PAAE1000/1001 | Revision 1.04

Liability Exclusion

We have tested the contents of this document regarding agreement with the hardware and software described. Nevertheless, there may be deviations and we do not guarantee complete agreement. The data in the document is tested periodically, however. Required corrections are included in subsequent versions. We gratefully accept suggestions for improvements.

This document is subject to changes without prior notice.

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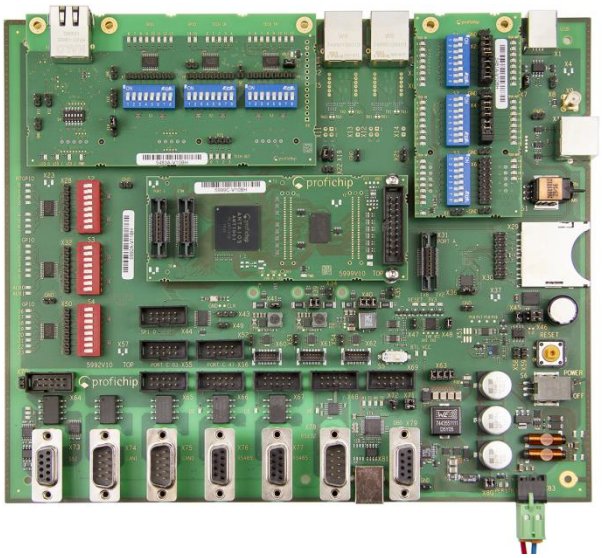
- 1x LP5481 (technology IO)



1x Debug PCB LP5966

1x USB cable

2x Ribbon cable

1x DC connector

2 Evaluation Board Overview

The ANTAIOS evaluation board consists of two basic components:

- The “mainboard” with all external interfaces, switches, LEDs, jumpers and power supply powered by 24 V DC
- The “coreboard” with the ANTAIOS ASIC itself, DDR2 SDRAM and JTAG/ETM interface

Figure 2-1 Mainboard

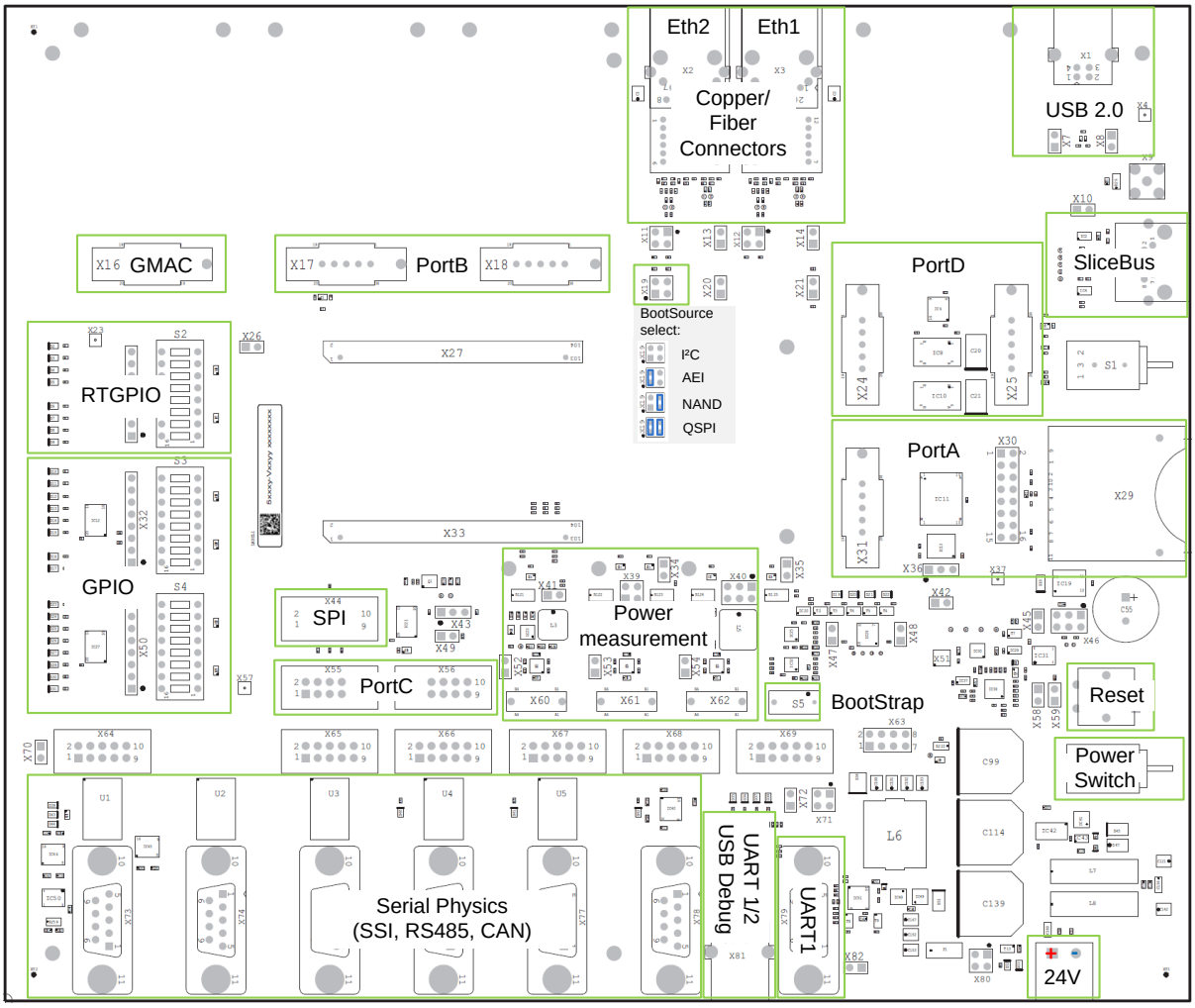
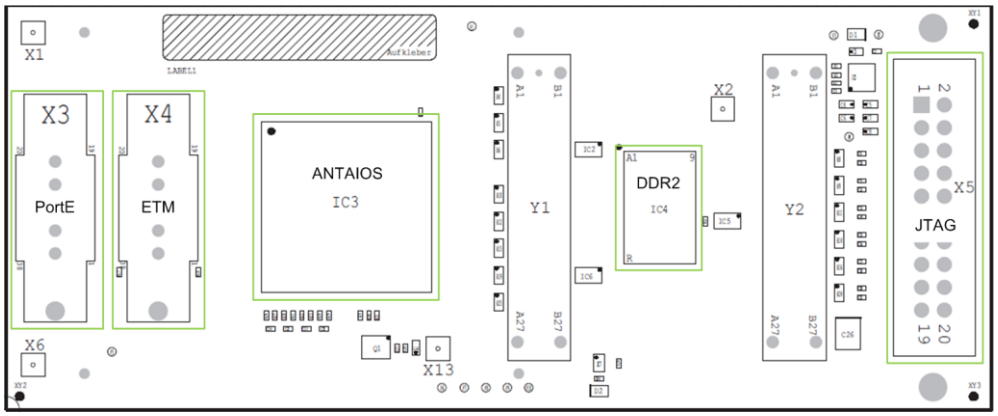


Figure 2-2 Coreboard



The coreboard is plugged onto the mainboard using the connectors X27 and X33.
To ensure the mechanical connection the coreboard is additionally fixed with two screws.

The functionality of the evaluation board can be extended by adding so called extension PCBs.
See chapter “5 - Extension PCBs” for more details.

3 Coreboard

3.1 ANTAIOS ASIC (IC3)

LP5998: TFBGA-380 (15x15 mm²) with 0.65 mm pitch.
LP5999: TFBGA-385 (19x19 mm²) with 0.80 mm pitch.

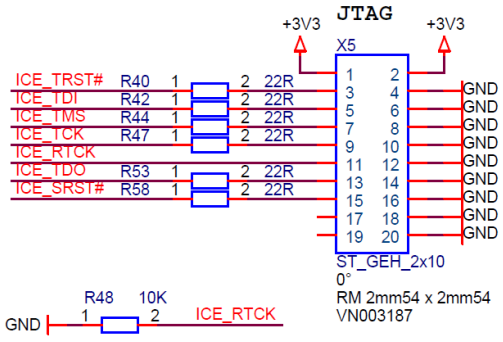
3.2 DDR2 SDRAM (IC4)

One Micron MT47H64M16NF-25E:M DDR2 memory chip is assembled on the coreboard.
The usable memory is 64 MByte of DDR2 SDRAM.
For debugging the DDR2 interface the contactless debug interface Keysight Soft Touch E5394A is supported on connectors Y1 and Y2 but not assembled by default.

3.3 JTAG Connector (X5)

The JTAG connector is used for connecting an in circuit debugger like “Power Debug” from Lauterbach for on-chip debugging. The maximum JTAG frequency is 48 MHz.

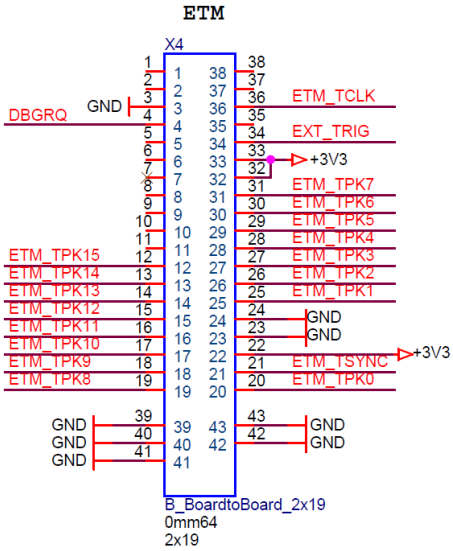
Figure 3-1 JTAG connector X5



3.4 ETM Connector (X4)

In conjunction with a trace device like “PowerTrace” from Lauterbach the ETM connector can be used to trace the program and data flow. The trace clock frequency is 144 MHz.

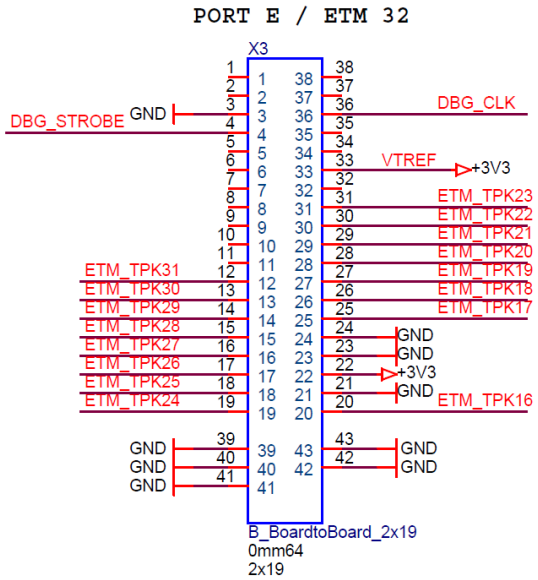
Figure 3-2 ETM connector X4



3.5 Port E - Debug Connector (X3)

Port E of ANTAIOS can be used to extend the ETM trace width from 16 to 32 data lines. Additionally 16 real time GPIOs or debug signals for Profibus Master, ARAC and PPU tracing can be driven to X3 by configuring the PinController of ANTAIOS.

Figure 3-3 Port E debug connector X3



PE0	DBG_DATA_0	ETM_TPK16
PE1	DBG_DATA_1	ETM_TPK17
PE2	DBG_DATA_2	ETM_TPK18
PE3	DBG_DATA_3	ETM_TPK19
PE4	DBG_DATA_4	ETM_TPK20
PE5	DBG_DATA_5	ETM_TPK21
PE6	DBG_DATA_6	ETM_TPK22
PE7	DBG_DATA_7	ETM_TPK23
PE8	DBG_DATA_8	ETM_TPK24
PE9	DBG_DATA_9	ETM_TPK25
PE10	DBG_DATA_10	ETM_TPK26
PE11	DBG_DATA_11	ETM_TPK27
PE12	DBG_DATA_12	ETM_TPK28
PE13	DBG_DATA_13	ETM_TPK29
PE14	DBG_DATA_14	ETM_TPK30
PE15	DBG_DATA_15	ETM_TPK31

3.6 Test Pads

Table 3-1 Coreboard test pads

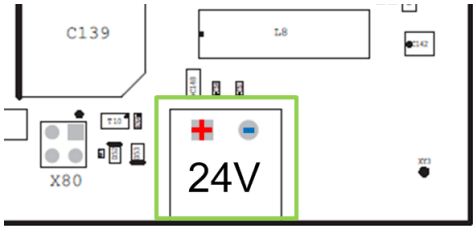
Pad	Description
P1	TEST3
P2	DDR_VREF
P3	PGOOD_VTT
P4	DDR_VTT
P5	TEST0
P6	1V2 ANTAIOS
P7	1V8 ANTAIOS
P8	GND
P9	1V8 DDR RAM
P10	3V3

4 Mainboard

4.1 Power Supply

The mainboard must be powered by a 24 V DC supply voltage connected to X83.

Figure 4-1 24 V DC connector X83

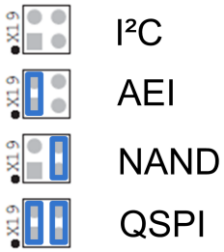


Depending on the extension PCBs used the evaluation board requires between 70mA and 220mA.

4.2 Boot Source Select (X19)

ANTAIOS supports booting from QSPI flash, NAND flash, 16 bit parallel interface (AEI) and I²C EEPROM. The boot source can be selected by setting appropriate jumpers to connector X19:

Figure 4-2 Bootsource selector X19

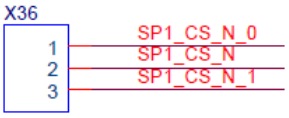


4.3 Port A - Quad SPI, NAND, SD/MMC

Depending on the PCB version of the mainboard either a QSPI flash and SD/MMC card slot (LP5992A) or a NAND flash (LP5992C) is assembled.

On PCB version 5992A one Micron N25Q064A13EF640 (3.3 V) 64 Mbit QSPI flash is assembled on the mainboard. Jumper X36 selects if CS0 or CS1 of ANTAIOS QSPI controller is driven to the QSPI flash.

Figure 4-3 QSPI CS selector X36



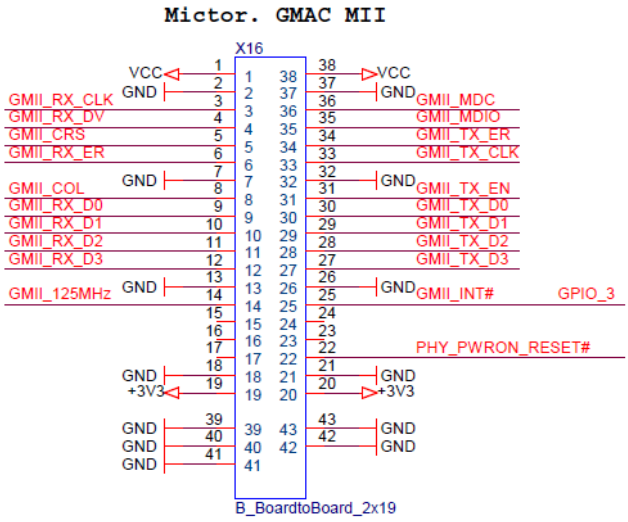
On PCB version 5992C one Micron MT29F8G08ABACAH4 (3.3V) 8 Gbit NAND flash is assembled on the mainboard.

4.4 Port B - Extension PCB Connectors for Gbit and External MII (X16, X17, X18)

The shared interfaces of ANTAIOS like external MII and GMII are accessible through various extension PCBs connected to MICTOR connectors.

Using only X16 the internal Gbit MAC can be operated in 10/100 Mbit mode.

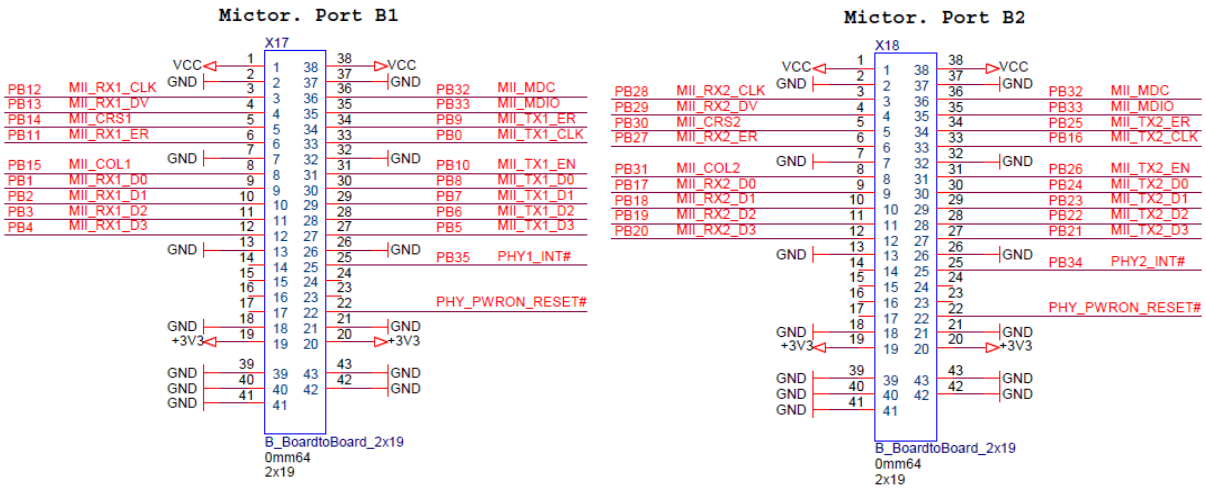
Figure 4-4 MII interface of internal GMAC X16



If the GMAC should be operated in the 1000 Mbit mode the user has to connect the extension PCB LP5483. This extension PCB connects the additional GMII signals from Port B on X17 to the Marvell 88E1119R Gbit PHY.

Port B of ANTAIOS additionally features the both external MII signals from the RT Ethernet switch. The 36 signals of Port B are connected to the MICTOR connectors X17 and X18:

Figure 4-5 External MII connectors X17 and X18



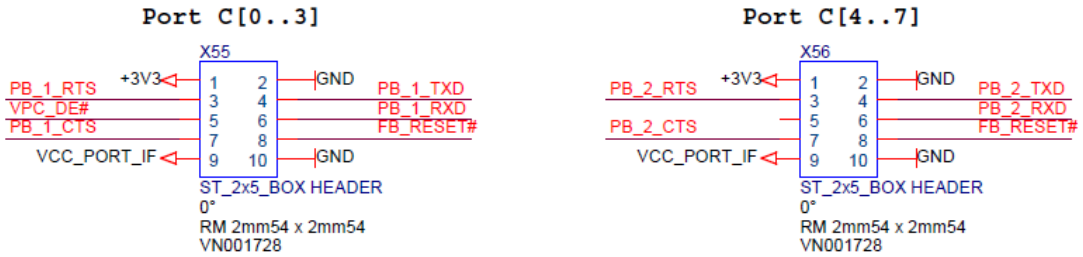
Please note that the TechIO and GPIO functions can't be used with the extension PCB version 5483A-V10. The TechIO functionality of PortB_v4 can be used by connecting the TechIO extension PCB LP5484 to X17 and X18.

If the internal PHYs of ANTAIOS are not used up to three 10/100 Mbit PHYs can be connected to X16, X17 and X18. The external PHY1 interrupt is connected to GPIO(6), external PHY2 interrupt is connected to GPIO(7).

4.5 Port C – VPC, UART, CAN, PBM and GPIO(X55, X56)

The eight data lines of Port C (VPC, UART 2, CAN 1/2, PBM 1/2 and GPIOs) are driven to two 2x5 pin headers and can be connected to the appropriate physics and D-sub connectors via ribbon cable.

Figure 4-6 Port C box header X55 and X56



4.6 Port D - Asynchronous External Interface (AEI), GPIOs, UART and TechIO

Port D of ANTAIOS can be used as asynchronous external interface (AEI) in master and slave mode, digital inputs and outputs with technology functionality and GPIOs and UART2.

All signals of Port D are driven to the MICTOR connectors X24 and X25. There are two special extension PCBs for Port D available which allow the usage of the TechIO or GPIO/UART2 functionality of Port D.

If no extension PCB is connected to X24 and X25 ANTAIOS can access an address range of up to 2 Mbyte using the asynchronous external interface (AEI) and two chip selects CS0 and CS1.

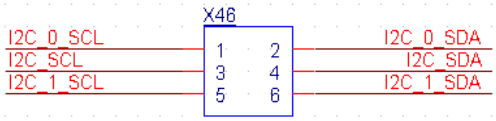
CS0: Used in master mode to connect to slave board (e.g. another ANTAIOS evaluation board) with the two MICTOR connectors of Port D.

CS1: connected to two Cypress CY14B108N-BA25XI 512k x 16 nvSRAM chips.
Note that the nvSRAM is not available as soon as any extension PCB is connected to Port D.

4.7 I2C

ANTAIOS features two I²C channels. I²C 1 is shared with GPIO 4/5 on Port F and I²C 2 is placed on Port C, also shared with other interfaces (see chapter 4.5). Two I²C devices are assembled on the mainboard, a 64 Kbit EEPROM (CAT24WC64) and a RTC (RTC-8564JE). The user has to choose which I²C channel should be used to access the I²C bus (I2C_SDA, I2C_SCL) of the mainboard by setting jumper X46:

Figure 4-7 I²C channel selector



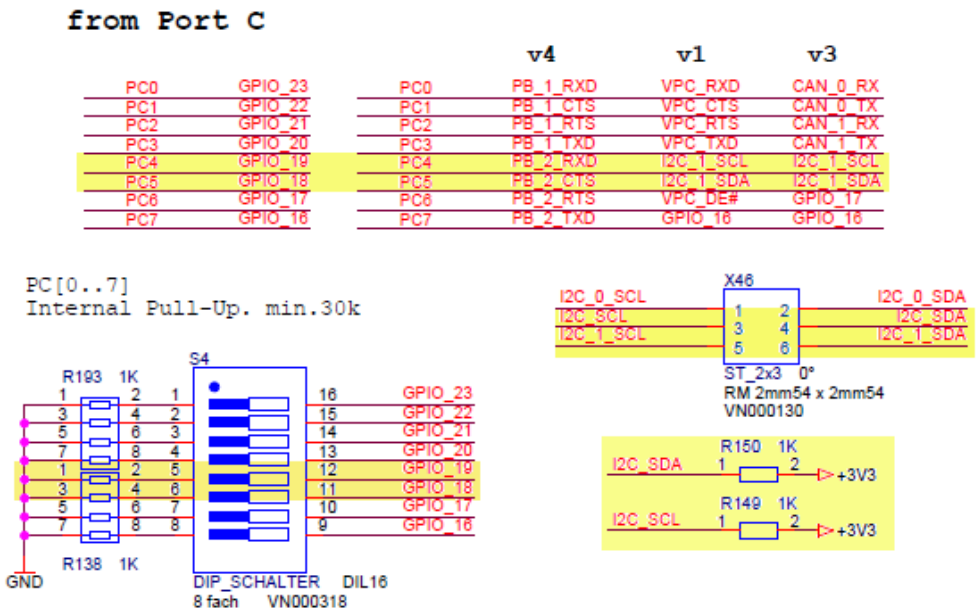
Please note that the numbering of the interfaces in the schematic differs.

Table 4-1 Naming of I²C interfaces

Interface (jumper setting)	Documentation	Schematic
1st I²C interface (1-3 and 2-4)	I²C 1	I2C_0
2nd I²C interface (3-5 and 4-6)	I²C 2	I2C_1

When using the I²C 2 interface at Port C, the DIP switch S4 must be set to OFF for the lines of GPIO18 and GPIO19. Otherwise 1 kΩ pull-down resistors are switched on, which competes against the I²C 1 kΩ pull-ups that are coupled via X46.
Same problem exists with the I²C 1 interface on Port F. Here the DIP switch S3 must be set to OFF for the lines of GPIO4 and GPIO5.

Figure 4-8 pull-up / pull-down conflict shown on the example of I²C 2 interface



Level of lines from the I²C interfaces are visible via LEDs. Signals can be accessed on pin headers X32 (I²C 1) and X50 (I²C 2). The 2nd interface is routed to the box header X56 additionally.

To enable write accesses to the CAT24WC64 64 Kbit EEPROM the user has to shorten jumper X45.

4.8 UART 1/2 and USB to serial converter

The two serial interfaces UART 1 and UART 2 can be routed to a 1000 kbps RS-232 transceiver (SP3232EU) or a dual USB to serial UART converter IC (FT2232D).

The USB to serial UART converter allows serial communication with UART 1/2 over USB without the need of a serial interface on the PC. The FT2232D requires USB drivers available free from http://www.ftdichip.com which are used to make the FT2232D appear as two virtual COM ports on the host PC. This allows the user to communicate with the USB interface via a standard PC serial emulation port (for example TTY).

Note: UART 1 is mapped to the virtual COM port with the higher number and UART 2 to the one with the lower number.

Jumper X72 selects if UART 1 uses the D-sub or USB debug connector.
When X72 is left open, UART 1 is driven to the D-sub connector X79.
If X72 is shortened the communication is done using the USB debug connector X81.

As UART 2 is shared via the PinController users can choose to use UART 2 either on Port C or Port D (extension PCB LP5482A-V10 needed) by connecting the headers according to the following table. No additional jumper settings are needed.

Table 4-2 UART 2 to connector configuration

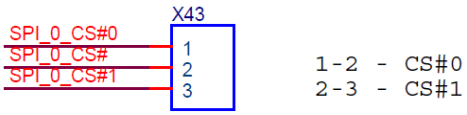
UART2 on	to connector	connect with ribbon cable
Port C	D-sub (X78)	X55 ↔ X68
	Debug USB (X81)	X55 ↔ X69
Port D	D-sub (X78)	X8(LP5482A-V10) ↔ X68
	Debug USB (X81)	X8(LP5482A-V10) ↔ X69

4.9 SPI

The Single SPI channel is directly connected to a 2x5 pin box header and can be used in master or slave mode, e.g., for connecting two ANTAIOS evaluation boards with a ribbon cable.

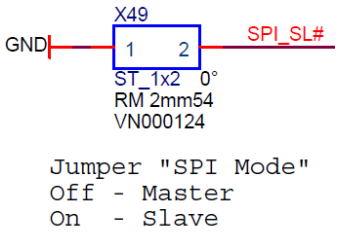
As the SPI controller offers two chip selects the user can choose if SPI_CS#0 or SPI_CS#1 should be driven to the box header by setting jumper X43:

Figure 4-9 SPI0 CS selector



To use the SPI channel in slave mode the user has to shortcut jumper X49:

Figure 4-10 SPI master/slave selector



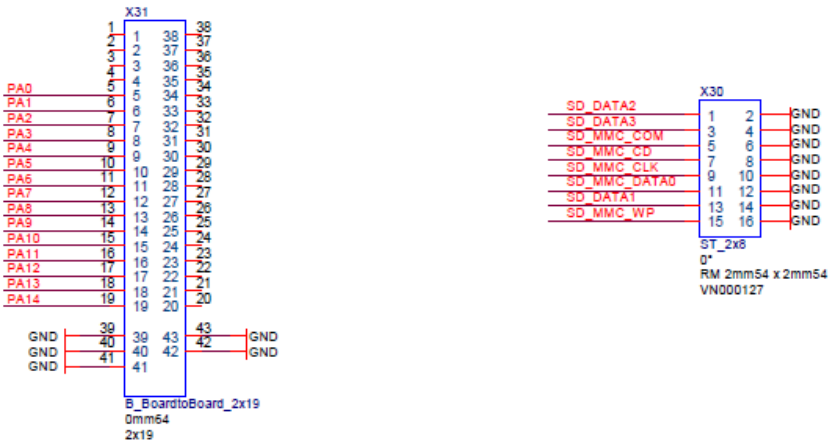
4.10 Test pads and debug connectors X31, X30, X50

Table 4-3 Test pads mainboard

Pad	Description
P1	TX2-
P2	TX2+
P3	TX1-
P4	TX1+
P5	RX2+
P6	RX2-
P7	RX1+
P8	RX1-
P9	Slicebus NDLI
P10	GND
P11	Slicebus ALARM
P12	GND
P13	Slicebus MDLO
P14	GND
P15	32 MHz ASIC clock soucre
P16	Power Analog0
P17	Power Cout
P18	Power Run#
P19	Power Boost
P20	EN_3V3
P21	PG_3V3
P22	I2C SCL
P23	I2C SDA
P24	EN_1V2
P25	EN_1V8
P26	Powergood 3V3
P27	Powergood 1V8
P28	Powergood 1V2
P29	Powergood VCC
P30	I_Shunt

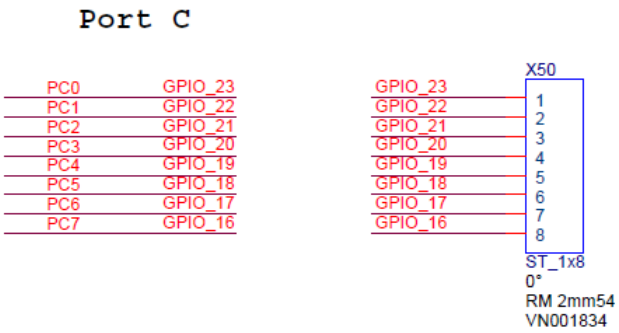
All 15 signals of Port A are driven to debug connector X31, the SD card signals are additionally connected to X30:

Figure 4-11 Port A debug connector X30 and X31



All eight signals of Port C are driven to 1x8 pin header X50:

Figure 4-12 Port C debug connector X50



4.11 Board to Board connectors (X27, X33)

The ANTAIOS coreboard is connected to the board to board connectors X27 and X33 and must be secured with two screws.

Figure 4-13 Board to board connectors X27 and X33

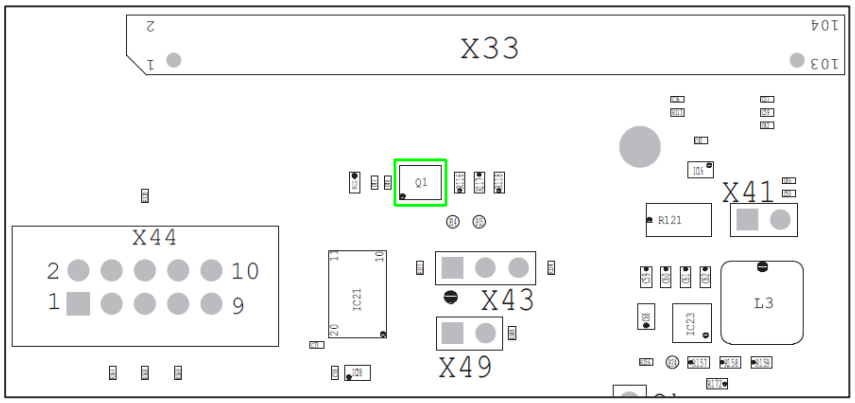
4.12 Boundary Scan (X22)

Placing a jumper on X22 activates the boundary scan mode of ANTAIOS.
For normal operation leave X22 open.

4.13 32 MHz clock source

The evaluation board mainboard PCBs LP5992A up to version V11 use a programmable crystal oscillator as 32 MHz clock source for the ANTAIOS ASIC.

Figure 4-14 Crystal oscillator Q1 as 32 MHz clock source



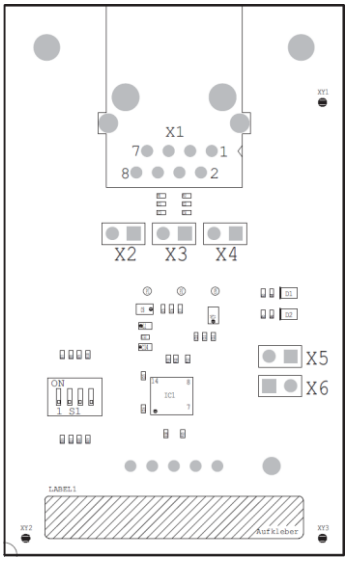
Please note that the use of programmable crystal oscillators will induce a considerable long-term jitter. For production devices a fixed frequency crystal oscillator should be used to reduce the long term jitter to a minimum.
See ANT1000_ANT1001_Datasheet.pdf for more details about jitter.

5 Extension PCBs

5.1 LP5480, ExtPHY_TI

Extension PCB for PortB_v1 with TI TLK106L 10/100 Mbit PHY.

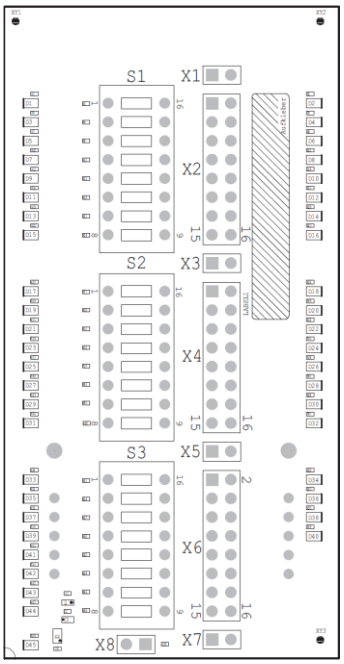
Figure 5-1 Extension PCB LP5480



5.2 LP5481, TechIO_Dv4

Extension PCB for PortD_v4 for technology functions.

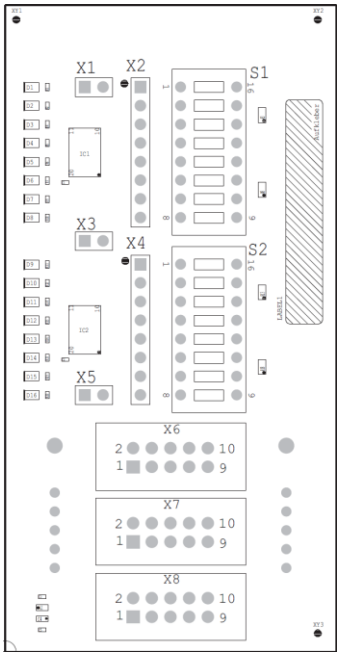
Figure 5-2 Extension PCB LP5481



5.3 LP5482, SerialD

Extension PCB for PortD_v3 for GPIOs, UART2, VPC and CAN 1/2

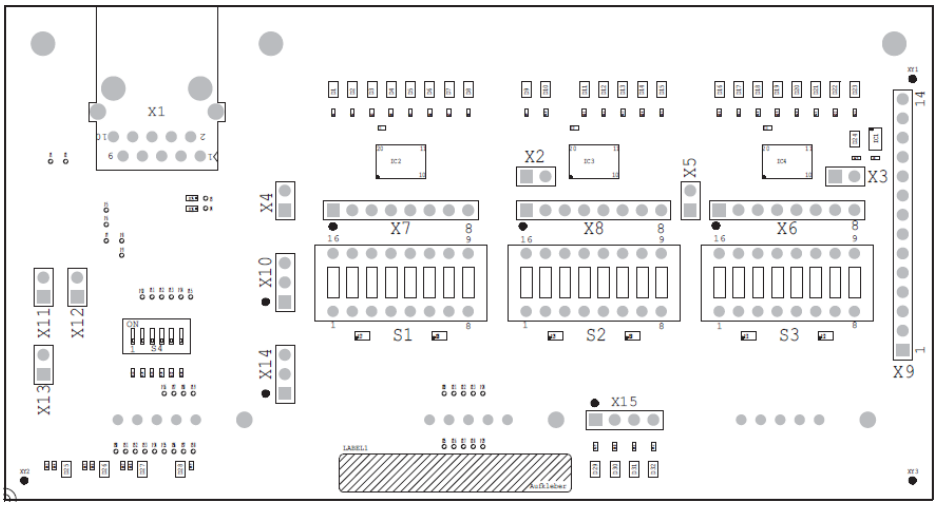
Figure 5-3 Extension PCB LP5482



5.4 LP5483, GPHY

Extension PCB for Gbit on PortB_v2/3 with Marvell 88E1119R 10/100/1000 Mbit PHY.
For proper operation pins 2 and 3 of jumper X14 must be shortened.

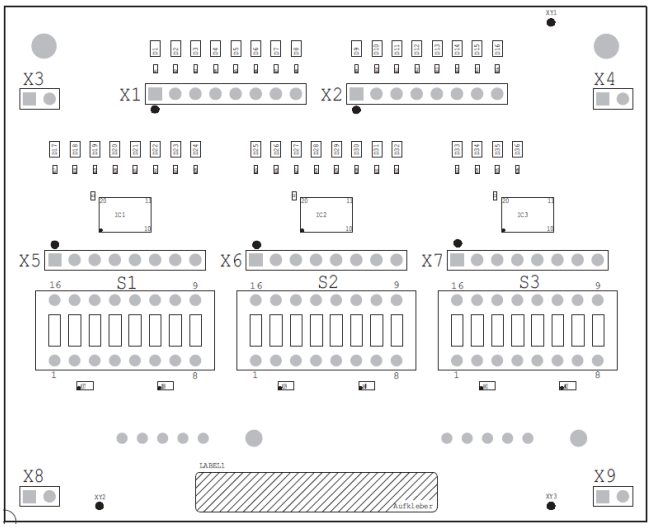
Figure 5-4 Extension PCB LP5483



5.5 LP5484, TechIO_Bv4

Extension PCB for PortB_v4 for technology functions.

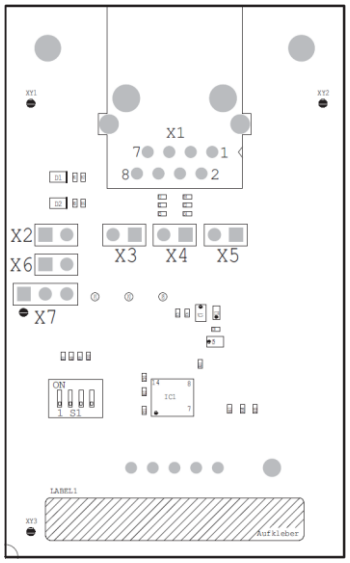
Figure 5-5 Extension PCB LP5484



5.6 LP5485, ExtPHY_MC

Extension PCB for PortB_v1 with Micrel KSZ8081MNXI 10/100 Mbit PHY.

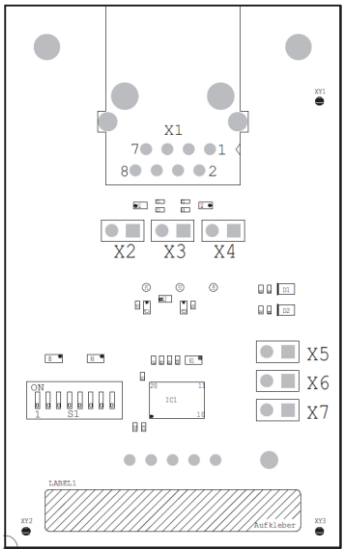
Figure 5-6 Extension PCB LP5485



5.7 LP5486, ExtPHY_BC

Extension PCB for PortB_v1 with Broadcom BCM5241A1IMLG 10/100 Mbit PHY.

Figure 5-7 Extension PCB LP5486



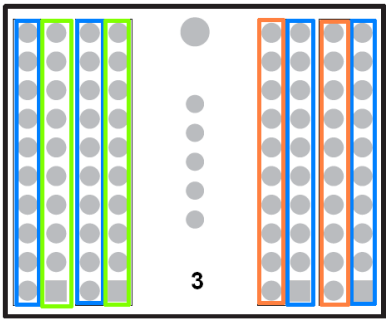
5.8 LP5487, BroadR

Broadcom BCM89810, PortB_v1
This schematic is not yet finished.

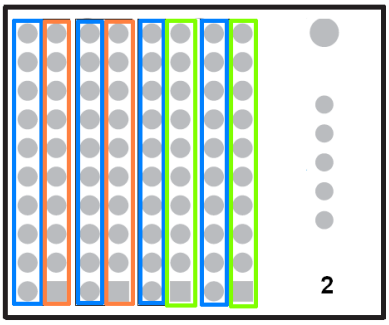
5.9 Debug PCB LP5966C

Debug PCB for connecting to any MICTOR connector on the ANTAIOS evaluation board. There are three different versions of the MICTOR PCB 1, 2 and 3 which differ in the placement and orientation of the MICTOR connector and header pins.

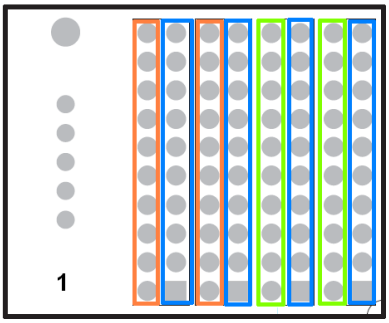
Figure 5-8 Debug PCB LP5966C



GND	3/CLKe		GND	3/CLKe	①		36/CLKo		GND	36/CLKo	
	5/D14e			4/D15e			35/D15o			34/D14o	
	7/D12e			6/D13e	o		33/D13o			32/D12o	
	9/D10e			8/D11e	o		31/D11o			30/D10o	
	11/D8e			10/D9e	o		29/D9o			28/D8o	
	13/D6e			12/D7e	o		27/D7o			26/D6o	
	15/D4e			14/D5e			25/D5o			24/D4o	
	17/D2e			16/D3e			23/D3o			22/D2o	
	19/D0e			18/D1e	3		21/D1o			20/D0o	



GND	36/CLKo		36/CLKo		GND	3/CLKe		GND	3/CLKe	①
	35/D15o		34/D14o			4/D15e			5/D14e	
	33/D13o		32/D12o			6/D13e			7/D12e	o
	31/D11o		30/D10o			8/D11e			9/D10e	o
	29/D9o		28/D8o			10/D9e			11/D8e	o
	27/D7o		26/D6o			12/D7e			13/D6e	o
	25/D5o		24/D4o			14/D5e			15/D4e	
	23/D3o		22/D2o			16/D3e			17/D2e	
	21/D1o		20/D0o			18/D1e			19/D0e	2



①	36/CLKo		36/CLKo		3/CLKe		3/CLKe	
	35/D15o		34/D14o		5/D14e		4/D15e	
o	33/D13o		32/D12o		7/D12e		6/D13e	
o	31/D11o	GND	30/D10o	GND	9/D10e	GND	8/D11e	GND
o	29/D9o		28/D8o		11/D8e		10/D9e	
o	27/D7o		26/D6o		13/D6e		12/D7e	
	25/D5o		24/D4o		15/D4e		14/D5e	
	23/D3o		22/D2o		17/D2e		16/D3e	
1	21/D1o		20/D0o		19/D0e		18/D1e	

The left part of **Fehler! Verweisquelle konnte nicht gefunden werden.** shows the various locations of the 8x 10 pin headers, all pins marked in blue are connected to GND.

The right side shows which pin on the debug PCB corresponds with which pin on the MICTOR connector on the mainboard, coreboard or extension PCB.

6 Order Information

Table 6-1 Order Information

PCB Number	Description	Port	Order Number
LP5992	ANTAIOS Evaluation Mainboard Copper	--	PAAE1010
LP5998	ANT1000 ANTAIOS Coreboard BGA 15x15 mm²	--	PAAE1000
LP5999	ANT1001 ANTAIOS Coreboard BGA 19x19 mm²	--	PAAE1001
LP5480	External PHY TI TLK106L	B_v1	PAAE1150
LP5481	TechIO	D_v4	PAAE1151
LP5482	UART, GPIOs, CAN	D_v3	PAAE1152
LP5483	External Gbit PHY Marvell 88E1119R	B_v2 / B_v3	PAAE1153
LP5484	TechIO	B_v4	PAAE1154
LP5485	External PHY Micrel KSZ8081MNXI	B_v1	PAAE1157
LP5486	External PHY Broadcom BCM5241A1IMLG	B_v1	PAAE1158
LP5487	External PHY Broadcom BCM89810	B_v1	PAAE1156
LP5966	Debug PCB for MICTOR connectors	--	PAAE1159

7 Revision History

Table 7-1 Revision history

Version	Date	Remarks
V0.01	28.10.2016	First draft version
V0.02	17.11.2016	Changed to new template
V0.03	22.12.2016	Renamed to PAAE1100/1101 Evaluation Kit
V0.04	23.12.2016	Added note about virtual COM port mapping when using the onboard serial to USB converter
V0.05	10.02.2017	Added oscillator remarks
V1.00	27.02.2017	First release
V1.01	19.05.2017	Changed document title
V1.02	20.09.2017	Corrected some typos
V1.03	01.10.2019	New document design
V1.04	04.08.2021	Added note about usage of port C for I²C

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